CLAIMS

What is claimed is:

1. A method for selectively plating recesses in a semiconductor substrate which comprises:

providing a semiconductor substrate;

providing at least one major surface thereof with recesses and providing electrical insulating layer over said at least one major surface and in said recesses;

forming a conductive barrier over said insulating layer;

forming a plating seed layer over said barrier layer;

depositing and patterning a photoresist layer over said plating seed layer for planarizing the insulated horizontal portions between recesses and for protecting said plating seed layer within said seed layer during subsequent planarizing;

then planarizing said insulated horizontal portions by removing the horizontal portions of said seed layer between recesses; removing the photoresist remaining in said recesses; and then electroplating the patterned seed layer with a conductive metal using said barrier layer to carry the current during said electroplating to thereby only plate on said seed layer.

2. The method of claim 1 wherein said conductive barrier is provided by sputter depositing a layer of tantalum nitride on said insulating layer and then sputter depositing a layer of tantalum on said tantalum nitride layer.

3. The method of claim 1 wherein said conductive barrier is alpha-tantalum.

4. The method of claim 2 wherein said conductive barrier is alpha-tantalum.

5. The method of claim 4 wherein the electroplating comprises electroplating copper.

6. The method of claim 3 wherein the electroplating comprises electroplating copper.

7. The method of claim 1 wherein said conductive barrier is provided by sputter depositing a layer of tantalum on said insulating layer and then sputter depositing a layer of nitrides of tantalum on said tantalum layer.

8. The method of claim 7 wherein said conductive barrier is provided by sputter depositing a layer of nitride of tantalum on said insulating layer and then sputter depositing a layer of tantalum on said tantalum nitride layer, such that the tantalum is in the alpha phase.

9. The method of claim 8 wherein the electroplating comprises electroplating copper.

10. The method of claim 2 wherein said tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick.

11. The method of claim 1 wherein said seed layer is copper.

12. The method of claim 4 wherein said copper is deposited by sputter coating, CVD or electroless plating.

13. The method of claim 4 wherein said copper layer is about 4000 Å to about 20,000 Å thick.

14. The method of claim 1 wherein said horizontal portions of said seed layer between recesses is removed by chemical-mechanical polishing.

15. The method of claim 1 wherein said conductive metal is copper.

16. The method of claim 1 which further comprises removing said conductive barrier from horizontal portions between said recesses.

17. The method of claim 16 wherein said conductive barrier is removed by reactive ion etching.

18. A method for selectively plating recesses in a semiconductor substrate which comprises:

providing a semiconductor substrate;

providing at least one major surface thereof with recesses and providing electrical insulating layer over said at least one major surface and in said recesses;

forming a conductive barrier over said insulating layer;

depositing and patterning a photoresist layer over said barrier layer on field regions;

depositing a seedlayer wherein said seedlayer is continuous on the horizontal regions of the recesses in the insulator, but discontinuous on their surrounding walls;

exposing said barrier within the vicinity of the periphery of said major surface by edge bead removal of said seedlayer;

and then electroplating the patterned seed layer with a conductive metal using said barrier layer to carry the current during said electroplating to thereby only plate on said seed layer;

removing said resist by a lift-off process; and

removing exposed barrier.

19. The method of claim 18 wherein said conductive barrier is provided by sputter depositing a layer of tantalum nitride on said insulating layer and then sputter depositing a layer of tantalum on said tantalum nitride layer.

20. The method of claim 19 wherein said conductive barrier is alpha-tantalum.

21. The method of claim 5 wherein the electroplating comprises electroplating copper.

22. The method of claim 10 wherein said tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick.

23. The method of claim 18 wherein said conductive metal is copper.

24. The method of claim 18 wherein said photoresist layer ~~is about 1.5 to about 50 Å thick.~~

25. A semiconductor structure comprising a semiconductor substrate; recesses located in at least one major surface of said semiconductor substrate; electrical insulating layer over said at least one major surface and in said recesses; a conductive barrier over said insulating layer; a plating seed layer located over said conductive barrier within said

recesses only; and an electroplated conductive metal in said recesses.

26. The semiconductor structure of claim 25 wherein said barrier comprises a layer of tantalum nitride adjacent said insulating layer and a layer of tantalum above said tantalum nitride layer.

27. The semiconductor structure of claim 26 wherein said tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick.

28. The semiconductor structure of claim 25 wherein said seed layer is copper.

29. The semiconductor structure of claim 28 wherein said copper is sputtered copper.

30. The semiconductor structure of claim 28 wherein said copper is about 4000 to about 20,000 Å thick.

31. The semiconductor structure of claim 25 wherein said electroplated conductive metal is copper.